EE

HIGH SPEED DIGITAL TRANSMISSION

Chairman: I. Mack—Naval Research Lab.

Session Abstract: The session, which includes 4 full length papers, deals with the timely and important topic of data transmission by high speed digital systems. The first paper describes a marriage of both silicon and GaAs technologies, combining the best features of both, to achieve 4.5 GBIT/S processing.

Next, an invited paper surveys sources of noise in high speed digital systems, discusses its characterization and specification, and provides design methodology and examples for minimizing noise effects.

The session continues with a description of the design and operation of high speed QPSK modulators and demodulators which are subharmonically pumped, and provide error rates of less than 10^{-11} at data rates of 1.5 GBIT/S at a 13 GHz carrier frequency.

Finally, the session ends with a description of a digital radio link which includes a novel direct division phase locked loop operating at the 22 GHz carrier frequency.

8:30 am–10:00 am, May 27, 1988
Jacob Javits Convention Center, Hall 1E
Room 3